AF/2664

Docket No.: 64965-057

PATENT #16
1-13-03
A2

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

| | | |
|---|---|---|
| In re Application of | : | |
| John CHIANG, et al. | : | |
| Serial No.: 09/304,964 | : | Group Art Unit: 2664 |
| Filed: May 05, 1999 | : | Examiner: Kwang Bin YAO |

For: DYNAMIC TIME SLOT ALLOCATION IN INTERNAL RULES CHECKER SCHEDULER

ok
1/14/03

**TRANSMITTAL OF REPLY BRIEF**



Commissioner for Patents
Washington, DC 20231

Sir:

Submitted herewith in triplicate is Appellant Reply Brief in response to the Examiner's Answer mailed November 14, 2002.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Alexander V. Yampolsky
Registration No. 36,324

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 JAH:AVY:ed
Facsimile: (202) 756-8087
**Date: January 9, 2003**

Docket No.: 64965-057 PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**


In re Application of :

John CHIANG, et al. :

Serial No.: 09/304,964 : Group Art Unit: 2664

Filed: May 05, 1999 : Examiner: Kwang Bin YAO

For: DYNAMIC TIME SLOT ALLOCATION IN INTERNAL RULES CHECKER SCHEDULER



**REPLY BRIEF**

Commissioner for Patents
Washington, DC 20231

Sir:

This Appeal Brief is submitted in response to the Examiner's Answer mailed November 14, 2002.

First, in the Examiner's Answer, the Examiner incorrectly indicated that the Appeal Brief does not contain a statement identifying the related appeals and interferences. However, page 1 of the Appeal Brief of September 10, 2002 contains a statement that no other appeals or interferences are known to the Appellant, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Further, as discussed in the Appeal Brief, claims 2-11 and 13-18 have been rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. (U.S. 5,771,234).

In particular, **independent claim 2,** among other features, recites logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one

selected transmit port for each data packet, and a scheduler interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports. The claim requires the scheduler to be configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry.

In the Office Actions, the Examiner did not point out specifically wherein Wu et al. discloses the claimed scheduler configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry.

In the Examiner's Answer, the Examiner contends that "Wu et al. **explicitly** discloses an example in FIG. 4 of scheduling time slots to different memories...." Then, the Examiner states that "the scheduling directly **implies** there is a request for a memory when there are data cells available for transmission."

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989).

It appears that the Examiner admits that the reference does not expressly describes the claimed scheduler configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry.

In the event the Examiner relied upon inherency without expressly indicating such reliance, the Examiner should be aware that inherency requires certainty, not speculation. ***In re Rijckaert***, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); ***In re King***, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); ***W. L. Gore & Associates, Inc. v. Garlock, Inc.***, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); ***In re***

***Oelrich***, 666 F.2d 578, 212 USPQ 323 (CCPA 1981); ***In re Wilding***, 535 F.2d 631, 190 USPQ 59 (CCPA 1976). To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. ***In re Robertson***, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

The Examiner provided no factual basis upon which to conclude that the reference discloses the claimed scheduler configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry

Instead, the Examiner discussed a memory access scheme disclosed in the reference.

Further, **independent claim 8,** among other features, recites logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet. The claim requires the logic circuitry to comprise ingress rules logic for receiving the data block to check whether the corresponding data packets are received with an error.

In the Office Actions, the Examiner did not point out wherein Wu discloses the claimed ingress rules logic.

In the Examiner's Answer, the Examiner disagrees with the Appellant's statement that Wu does not disclose the claimed ingress rules logic. However, instead of pointing out wherein the reference discloses the **ingress rules** logic, the Examiner discusses an error detection mechanism of Wu. The Examiner provided no reason to conclude that the Wu's error detection mechanism comprises ingress rules logic.

Further, **independent claim 13,** among other features recites the steps of transferring the data queues in successive time slots to logic circuitry for determining the at least one transmit port, and

dynamically allocating the time slots to the data queues in accordance with data traffic at the corresponding receive ports. The claim requires a data queue representing each of the receive ports to be assigned with at least one of the time slots.

In the Office Actions, the Examiner did not point out wherein Wu discloses that a data queue representing each of the receive ports is assigned with at least one of the time slots.

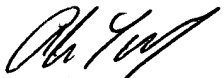
In the Examiner's Answer, the Examiner admits that Wu does not disclose this feature. In particular, the Examiner states that "each memory .... can be allocated to at least one time slot. Though some of the data cell in some timeslot ....is dropped since there is no time slot available for it, the memory ....can still be assigned at different time slots..." (page 8, lines 11-15 of the Examiner's Answer).

Accordingly, the Examiner's statement confirms that Wu does not disclose the invention claimed in claim 13 that recites that a data queue representing each of the receive ports is assigned with at least one of the time slots.

For the reasons advanced above, Appellant respectfully contends that the rejection of claims 2-11 and 13-18 as being anticipated under 35 U.S.C. § 102 is improper as the Examiner has not met the burden of establishing a *prima facie* case of anticipation.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



Alexander V. Yampolsky
Registration No. 36,324

600 13th Street, N.W.
Washington, DC 20005-3096
(202)756-8000 JAH:AVY:ed
Facsimile: (202)756-8087
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